

PG Interface (5 V Line Driver) Card "OPC-G1-PG22"

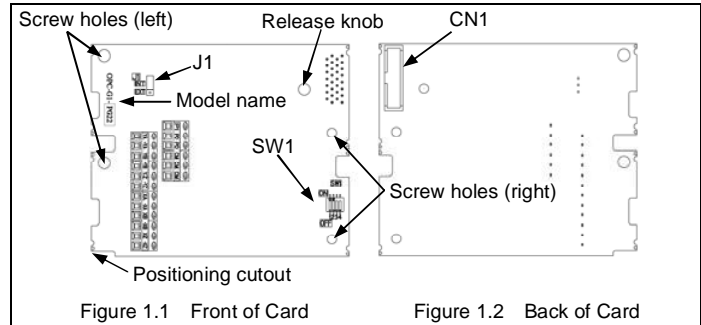
Thank you for purchasing this PG interface card containing 5 V line driver card (hereinafter called PG interface card), "OPC-G1-PG22." Mounting this card on your FRENIC-MEGA enables synchronous operation of two motors using PGs or frequency command entry by pulse train input.

- Note**
- Mounting this interface card disables the pulse train input function assigned to the inverter's [X7] terminal.
 - The FRENIC-MEGA has three option connection ports--A-, B-, and C-ports. Connect this PG interface card to the C-port. The A- and B-ports cannot accept this card. Mounting this card occupies also the B-port space so that any option card cannot be connected to the B-port.

1 Check that:

- (1) A PG interface card and four screws (M3 × 8) are contained in the package.
- (2) The PG interface card is not damaged during transportation--no defective devices, dents or warps.
- (3) The model name "OPC-G1-PG22" is printed on the PG interface card. (See Figure 1.1.)

If you suspect the product is not working properly or if you have any questions about your product, contact the shop where you bought the product or your local Fuji branch office.



2 Installation

⚠ WARNING ⚠

Before starting installation and wiring, turn OFF the power and wait at least five minutes for inverters with a capacity of 22 kW or below, or at least ten minutes for inverters with 30 kW or above. Make sure that the LED monitor and charging lamp are turned OFF. Further, make sure, using a multimeter or a similar instrument, that the DC link bus voltage between the terminals P(+) and N(-) has dropped to the safe level (+25 VDC or below).

Otherwise, electric shock could occur.

- (1) Remove the front cover from the inverter and expose the control printed circuit board (control PCB). The PG interface card can be connected to the C-port (CN6) only. (Figure 2.1)
 - To remove the front cover, refer to the FRENIC-MEGA Instruction Manual, Section 2.3. For inverters with a capacity of 30 kW or above, open also the keypad enclosure.
- (2) Insert connector CN1 on the back of the PG interface card (Figure 1.2) into the C-port (CN6) on the inverter's control PCB. Then secure the card with the four screws that come with the card. (Figure 2.3)

- Note** Check that the positioning cutout (Figure 1.1) is fitted on the tab (① in Figure 2.2) and connector CN1 is fully inserted (② in Figure 2.3). Figure 2.3 shows the PG interface card correctly mounted. Do not connect the interface card to the ports other than C-port. Doing so may damage the card.

- (3) Perform wiring to the PG interface card.
 - Refer to Section 3 "Wiring."
- (4) Put the front cover back into place.
 - To put back the front cover, refer to the FRENIC-MEGA Instruction Manual, Section 2.3. For inverters with a capacity of 30 kW or above, close also the keypad enclosure.

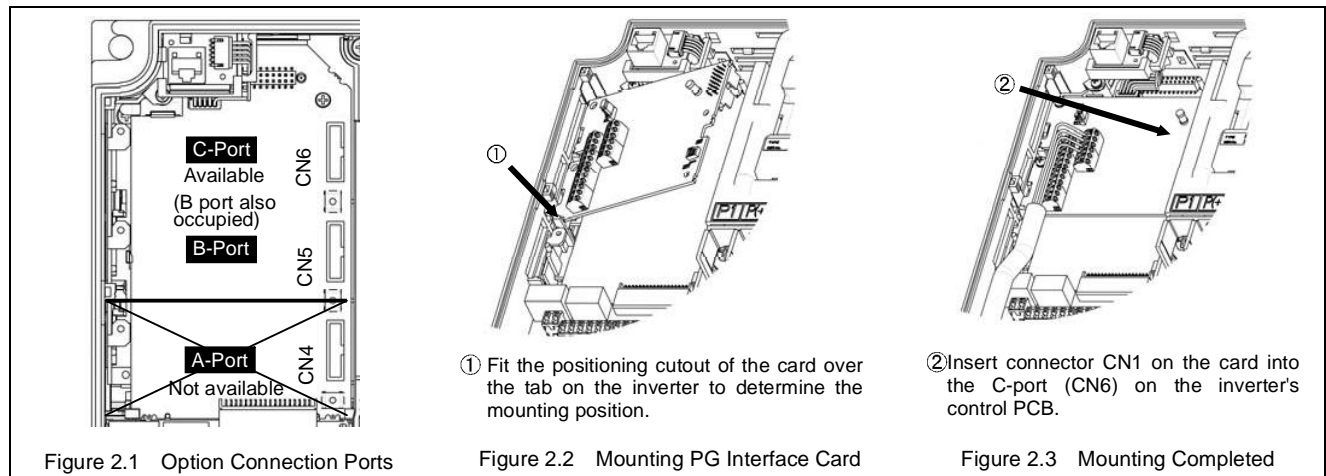


Figure 2.1 Option Connection Ports

Figure 2.2 Mounting PG Interface Card

Figure 2.3 Mounting Completed

3 Wiring

⚠ WARNING ⚠

In general, the covers of the control signal wires are not specifically designed to withstand a high voltage (i.e., reinforced insulation is not applied). Therefore, if a control signal wire comes into direct contact with a live conductor of the main circuit, the insulation of the cover might break down, which would expose the signal wire to a high voltage of the main circuit. Make sure that the control signal wires will not come into contact with live conductors of the main circuit.

Failure to observe these precautions could cause electric shock or an accident.

⚠ CAUTION ⚠

Noise may be emitted from the inverter, motor and wires.

Take appropriate measures to prevent the nearby sensors and devices from malfunctioning due to such noise.

An accident could occur.

Perform wiring to the PG interface card, referring to the "Terminal Allocation and Symbol Diagram" (Figure 3.1), "Terminal Specifications" (Table 3.1), "Internal Block Diagram" (Figure 3.2), and "Wiring Instructions" (Figure 3.3) given below.

For wiring between the PG interface card and the PG(s), use a shielded cable having a length of 100 m or below. It is recommended that the shielded layer be connected to the [CM] terminal on the card and be open at the PG side. If malfunctioning due to noise causes a problem, winding the shielded cable around a ferrite core by one or two turns may reduce the problem.

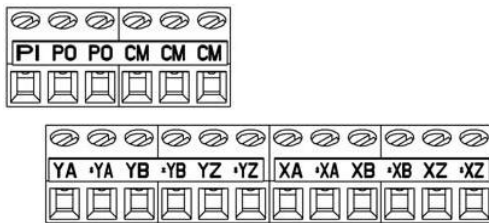


Figure 3.1 Terminal Allocation and Symbol Diagram

Table 3.1 Terminal Specifications

Terminal Size	M2
Tightening Torque	0.22 to 0.25 N·m
Recommended Wire *1	AWG16 to 24
Wire strip length	6 to 7 mm

*1 Insulated wires with allowable temperature of 105°C (UL-listed) are recommended.

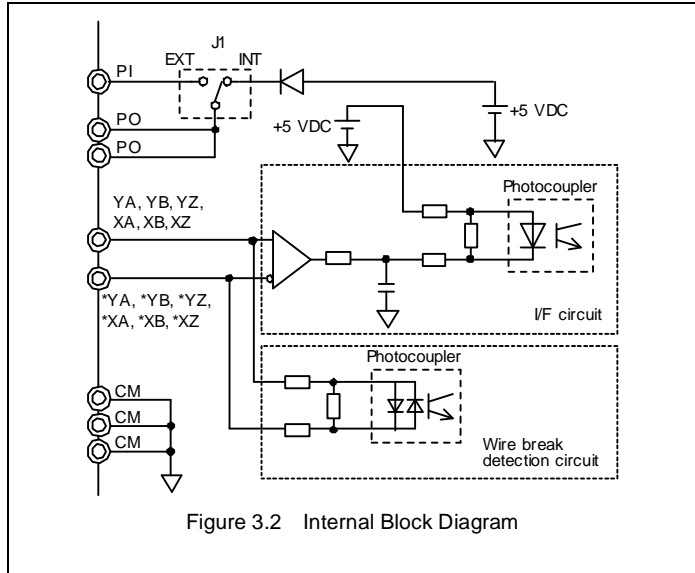
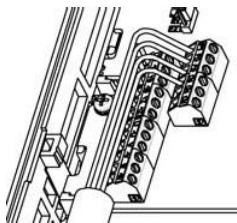


Figure 3.2 Internal Block Diagram

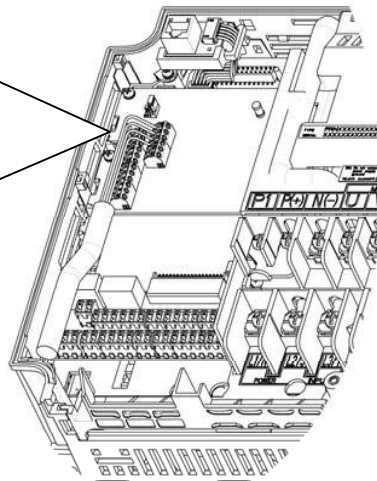


To prevent malfunctioning due to noise, separate the wires of the interface card as far apart as possible from those for the main circuits. Also, inside the inverter, bundle and fix the wires of the interface card so that they do not come into direct contact with the main circuit terminal block or other live parts of the main circuits.

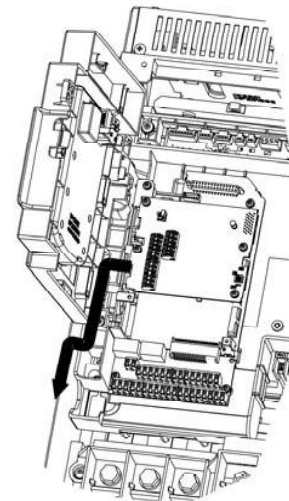
Connect the shielded layer to a [CM] terminal.
If [CM] terminals are lacking, share a single terminal with two wires and tighten them together.



Connecting the cable to terminals (magnified view)



In the case of 7.5 kW



In the case of 75 kW

Pass the wires from the PG interface card between the control circuit terminal block and the front cover.

Figure 3.3 Wiring Instructions

4 Specifications

Table 4.1 lists the specifications of the PG interface card.

Table 4.1 PG Interface Card Specifications

Item		Specifications
Applicable PG	Pulse resolution	20 to 3000 P/R
	Maximum response frequency	100 kHz
	Pulse output system	Line driver (Equivalent to 26C31 or 26LS31) Source current: +20 mA (max.), Sink current: -20 mA (max.)
	Maximum wiring length	100 m
PG power supply		+5 VDC \pm 10%, 300 mA or below *1

*1 When the PG current consumption exceeds 300 mA, use an external power supply.

5 Terminal Functions

Table 5.1 lists terminal symbols, names and functions of the option terminals on the PG interface card.

Table 5.1 Option Terminals and Their Specifications

Terminal symbol	Name	Functions
Power supply	PI	External power supply input *1 +5 VDC \pm 10% input *2 (A power supply to be connected should assure the PG current consumption or larger.)
	PO	Internal power supply output *4 +5 VDC -0% to +10%, 300 mA output *3
	CM	PG power common *5 Common terminal for power supply for PG (Equipotent with [CM] terminal of the inverter)
PG/pulse input	YA	YA(+) phase pulse input from slave PG Input terminal for A(+) phase signal fed back from the slave PG
	*YA	YA(-) phase pulse input from slave PG Input terminal for A(-) phase signal fed back from the slave PG
	YB	YB(+) phase pulse input from slave PG Input terminal for B(+) phase signal fed back from the slave PG
	*YB	YB(-) phase pulse input from slave PG Input terminal for B(-) phase signal fed back from the slave PG
	YZ	YZ(+) phase pulse input from slave PG Input terminal for Z(+) phase signal fed back from the slave PG
	*YZ	YZ(-) phase pulse input from slave PG Input terminal for Z(-) phase signal fed back from the slave PG
	XA	XA(+) phase pulse input from reference PG Input terminal for A(+) phase signal fed back from the reference PG
	*XA	XA(-) phase pulse input from reference PG Input terminal for A(-) phase signal fed back from the reference PG
	XB	XB(+) phase pulse input from reference PG Input terminal for B(+) phase signal fed back from the reference PG
	*XB	XB(-) phase pulse input from reference PG Input terminal for B(-) phase signal fed back from the reference PG
	XZ	XZ(+) phase pulse input from reference PG Input terminal for Z(+) phase signal fed back from the reference PG
	*XZ	XZ(-) phase pulse input from reference PG Input terminal for Z(-) phase signal fed back from the reference PG

*1 When the PG current consumption exceeds 300 mA, use an external power supply and set a jumper cap at the EXT side on jumper J1. (Refer to Section 6 "Configuration".)

*2 Use an external power supply whose rating meets the allowable voltage range of the PG. Regulate the external power supply voltage within the PI voltage range (upper limit +10%), taking into account the voltage drop caused by the PG-inverter wiring impedance. Or, use a wire with a larger diameter. (Refer to Table5.2)

*3 If the PO voltage level falls below the allowable voltage range of the PG due to voltage drop caused by PG-inverter wiring impedance, use an external power supply or a wire with a larger diameter.

*4 *5 The PG interface card has two [PO] terminals and three [CM] terminals, each of which is conducting inside the card.

Table 5.2 Recommended Wire Size

PG power supply requirements	Wiring length (m)				
	Up to 20	Up to 30	Up to 50	Up to 75	Up to 100
5 V \pm 10%, 300 mA	AWG24 (0.25 mm ²)	AWG22 (0.34 mm ²)	AWG20 (0.50 mm ²)	AWG18 (0.75 mm ²)	AWG16 (1.25 mm ²)

6 Configuration

6.1 Switching between internal and external power supplies for PGs

Before powering on the inverter, switch between internal and external power supplies for the PGs using jumper J1, referring to Table 6.1 and Figure 6.1.

Table 6.1 Internal and External Power Supplies for PGs

Power Supply	Short-circuit jumper J1 using a jumper cap
Internal power supply (Factory default)	At the INT side (Use the power supply with max. 300 mA load current.)
External power supply	At the EXT side Connect +5 VDC $\pm 10\%$ power to the [PI] terminal.

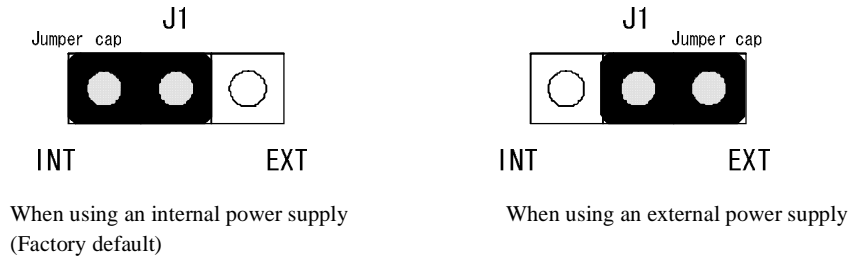


Figure 6.1 Configuration of Jumper J1

6.2 Enabling/disabling the wire break detection function with DIP SW1

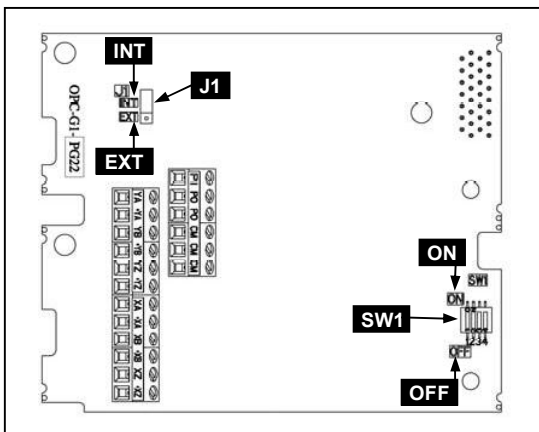
The PG interface card has a wire break detection function that detects wire breaks in the PG cable. It is possible to enable/disable this detection function in each of the YZ, XA, XB, and XZ phases. Please refer to Table 6.2 when enabling/disabling the detection function for each phase with the DIP SW1.

Note that the wire break detection function of the YA and YB phases is always enabled. When not using these phases, connect their respective (+) phases to the [PO] terminals and their respective (-) phases to the [CM] terminals.

Table 6.2 Enabling/Disabling the Wire Break Detection Function

Target	Selector No. on DIP SW1	Wire Break Detection Function *1	
		To enable (Factory default)	To disable
YZ phase	1	OFF	ON
XA phase	2	OFF	ON
XB phase	3	OFF	ON
XZ phase	4	OFF	ON

*1 When a particular signal line is not to be connected or not to be used even if connected, turn the corresponding selector to the ON position.



Note

- To move selectors on the DIP SW1, use a tool with a narrow tip (e.g., tweezers). Be careful not to touch other electronic parts, etc.
- Be sure to place the selector so that it contacts either side of the ON and OFF positions.

7 Drive Control

Table 7.1 shows the relationships among the drive control, inverter types, ROM versions, and PG(s).

For details about operation by pulse train input, refer to the FRENIC-MEGA Instruction Manual or User's Manual. For detailed configuration of synchronous operation, refer to the Synchronous Operation Manual that comes with the PG interface card.

Table 7.1 Drive Control, Inverter Types, ROM Versions, and Pulse Input from PG(s)

Drive Control		Inverter Type	Inverter Capacity	ROM Version	PG(s)/Pulse input	
					Slave PG (Y)	Reference PG (X)
F42/A14/b14/r14 *1		FRENIC-MEGA *3 FRN□□□G1□-□□□	Any capacity	3510 or later		
Pulse train input *2	0: V/f control with slip compensation inactive				--	Required
	1: Dynamic torque vector control				--	Required
	2: V/f control with slip compensation active				--	Required
	3: V/f control with speed sensor				Required	Required
	4: Dynamic torque vector control with speed sensor				Required	Required
	5: Vector control without speed sensor				--	Required
6: Vector control with speed sensor	Required				Required	
Synchronous operation	3: V/f control with speed sensor				Required	Required
	4: Dynamic torque vector control with speed sensor				Required	Required
	6: Vector control with speed sensor	Required	Required			

*1 For details about F42/A14/b14/r14 "Drive Control Selection," refer to the FRENIC-MEGA Instruction Manual.

*2 Pulse train generator of line driver type enables frequency control of PG-equipped motors.

*3 Boxes replace alphanumeric letters that represent inverter capacity, enclosure, power supply voltage, etc.

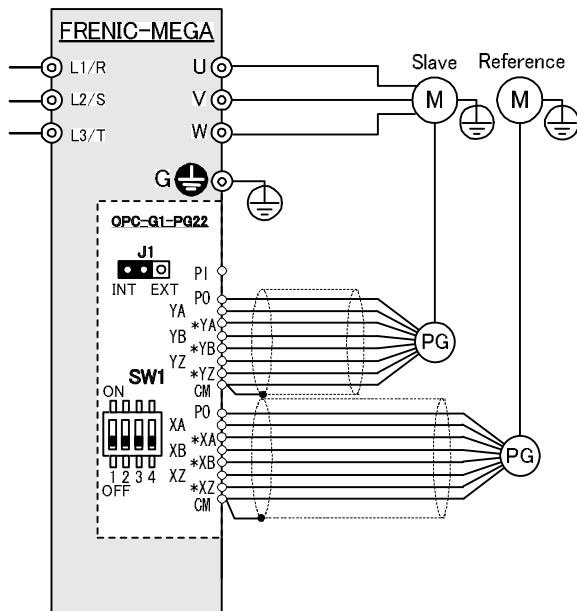
To check the inverter's ROM version, use Menu #5 "Maintenance Information 5_14" in Programming mode. For details, refer to the FRENIC-MEGA Instruction Manual, Chapter 3, Section 3.4.6 "Reading maintenance information."

Display on LED Monitor	Item	Description
5_14	Inverter's ROM version	Shows the inverter's ROM version as a 4-digit code.

7.1 Connection diagram examples for synchronous operation

Figure 7.1 shows the connection diagram examples enabling synchronous operation of the reference and slave motors.

When using inverter internal power supply.



When using external power supply.

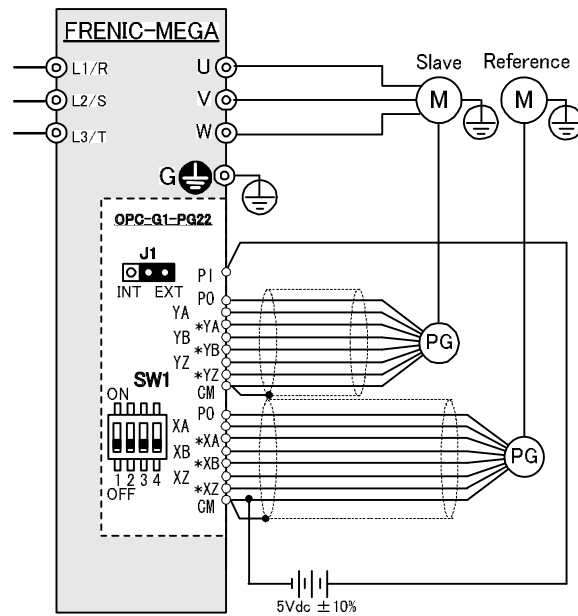


Figure 7.1 Connection Diagrams for Synchronous Operation

- For wiring between the PG and the inverter, use a shielded cable. It is recommended that the shielded layer be connected to the [CM] terminal on the card and be open at the PG side.
- If the wiring between the PG and the inverter is long, interference of A- and B-phases may cause PG signal malfunctions, resulting in abnormal noise or torque pulsation. In such a case, minimizing the wiring length (by reviewing the wiring route) or using a cable with smaller stray capacitance may reduce the problem.
- When using an inverter internal power supply, set a jumper cap at the INT side on jumper J1; when using an external power supply, at the EXT side.
- If malfunctioning due to noise causes a problem, winding the shielded cable around a ferrite core by one or two turns may reduce the problem.
- Mounting this interface card disables the pulse train input function assigned to the inverter's [X7] terminal.

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